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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,900	12/30/2003	Il-Goo Kim	8028-39 (SPX200211-0051US	7438

7590 06/28/2004

Frank Chau, Esq.
F. CHAU & ASSOCIATES, LLP
1900 Hempstead Turnpike
East Meadow, NY 11554

EXAMINER	
ROCCHEGIANI, RENZO	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/748,900	Applicant(s) KIM ET AL.	
	Examiner Renzo N. Rocchegiani	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 2-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. There is an inconsistency between the language of these claims and the claim upon which they depend. Claim 1 teaches, *inter alia*, "forming a via hole exposing the lower interconnection line". Yet, claim 2, recites that a via etch stop layer is formed over the interconnection line and that is not etched until after the sacrificial layer is removed. Thus, claim 2 contradicts instead of further limiting claim 1. This renders claim 2 indefinite. Claim 3 and 4 depend on claim 2 and thus are indefinite for the same reason.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 9-10 and 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,383,912 B1 (Chung et al.).

Chung et al. disclose a method of forming a via contact structure for an interconnect structure (col. 1, lines 15-20) comprising forming an intermetal dielectric (Fig. 2A) over the entire surface of an interconnect and forming a hard mask over the intermetal dielectric. (Fig. 2A) Chung et al. further disclose patterning the hard mask layer and the intermetal dielectric layer to form a via hole exposing the lower interconnection line. (Figs. 2B-2E) Furthermore, the process comprises the steps of forming a sacrificial layer (Fig. 2F) filling the via hole and on the hard mask layer and patterning the sacrificial layer and the hard mask layer to form a first sacrificial layer pattern having an opening that crosses over the via hole and a second sacrificial layer patter that remains in the via hole and to simultaneously form a hard mask pattern underneath the first sacrificial layer pattern (Fig. 2H) and partially etching the intermetal dielectric layer using the hard mask pattern and the sacrificial layer as etching masks (Fig. 2I) to form a trench crossing over the via hole and removing the second sacrificial layer pattern to expose the lower interconnection line. (Fig. 2I) Chung et al. further disclose that the hard mask may comprise a metal nitride such as titanium nitride. (col. 10, lines 31-39). The hard mask is later removed. (Fig. 2I). The via and trench are then filled with a metal and a diffusion barrier layer and the metal is then planarized. (Fig. 2J).

5. Claims 1-4, 6-12, 14-16, 18-24, and 26-28 arevrejected under 35 U.S.C. 102(e) as being anticipated by US Patent Publication No. 2003/0157806 A1 (Nagahara et al.).

For the purposes of this rejection ONLY, claim 1 is given an interpretation that overcomes the 112 rejection stated above so that the patentability with respect to prior art rejection of claims 2-4 may be addressed. Further, all claims dependent on claim 1 are being addressed giving claim 1 an interpretation consistent with claims 2-4. The 112 rejection still applies to claims 2-4 and claim 1 is rejected with respect to its proper interpretation in paragraphs 4, 7 and 8 together with some of the dependent claims.

Nagahara et al. disclose a method of forming a via contact structure for an interconnect structure [0004] comprising forming over the entire surface of an interconnect (item 8) an intermetal dielectric layer, comprising a lower intermetal dielectric layer (item 6), a SiC trench etch stop layer (item 5 and [0044]) and an upper intermetal dielectric layer (item 4), and forming a SiN or SiC or SiCN hard mask (item 3 and [0045]) over the intermetal dielectric layer. Nagahara et al. further disclose patterning the hard mask layer and the intermetal dielectric layer (items 4, 5 & 6) to form a via hole (Fig. 1A) exposing a SiCN via etch stop layer (item 7 and [0044]) that was deposited over the interconnection line (item 8) prior to the deposition of the intermetal dielectric (items 4, 5 & 6). Furthermore, the process comprises the steps of forming an HSQ sacrificial layer (item 2, [0062, 0063 and 0046]) filling the via hole and on the hard mask layer (See Figs. 1B and/or Fig. 8B) and patterning the sacrificial layer using a photoresists material, that is later removed, as a mask (item 1) and patterning the hard mask layer using the photoresist material and the sacrificial layer as masks (Fig. 1E and/or 8E) so as to form a first sacrificial layer pattern having an opening that crosses over the via hole and a second sacrificial layer patter that remains in the via hole (See

Figs. 1E and/or 8E) and to simultaneously form a hard mask pattern underneath the first sacrificial layer pattern (Figs. 1E and/or 8E) and etching the upper intermetal dielectric layer (item 4) using the hard mask pattern and the sacrificial pattern as etching masks (Fig. 1F and/or 8F) to form a trench crossing over the via hole and removing the second sacrificial layer pattern to expose the lower interconnection line. (Fig. 1G and/or 8G) Finally, the exposed via etch stop layer is removed so that the lower interconnection line is exposed. (Fig. 1G and/or 8G). Nagahara et al. further disclose that the via is filled with a metal layer that is planarized. (Fig. 1H and/or 8H). The hard mask layer 3 is removed simultaneously with the planarization of the metal layer. [0101]

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,383,912 B1 (Chung et al.).

As stated in paragraph 4 all the limitations of this claim have been met except for specifying that the hard mask layer is removed during or after the planarization step.

While Chung et al. disclose the removal of the hard mask layer prior to the filling of the trench, this limitation is rendered obvious to one with ordinary skill in the specific art to remove the hard mask layer during or after the planarization step solely in light of

Chung et al. since in general the transposition of process steps or the splitting of one step into two, where the processes are substantially identical or equivalent in terms of function, manner and result, was held to not patentably distinguish the processes. *Ex parte Rubin* 128 USPQ 159.

8. Claims 6-8, 11-12, 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,383,912 B1 (Chung et al.) in view of US Patent Publication No. 2003/0157806 A1 (Nagahara et al.).

As stated in paragraph 4, all the limitations of these claims have been met except for specifying that the intermetal dielectric layer is composed of multiple dielectric layers and that the sacrificial layer is formed of HSQ and it is patterned using a photoresist material.

Nagahara et al. teach a method of forming a via contact structure for an interconnect structure [0004] comprising forming over the entire surface of an interconnect (item 8) an intermetal dielectric layer, comprising a lower intermetal dielectric layer (item 6), a SiC trench etch stop layer (item 5 and [0044]) and an upper intermetal dielectric layer (item 4), and forming a SiN or SiC or SiCN hard mask (item 3 and [0045]) over the intermetal dielectric layer. Nagahara et al. further teach patterning the hard mask layer and the intermetal dielectric layer (items 4, 5 & 6) to form a via hole (Fig. 1A). Furthermore, the process comprises the steps of forming an HSQ sacrificial layer (item 2, [0062, 0063 and 0046]) filling the via hole and on the hard mask layer (See Figs. 1B and/or Fig. 8B) and patterning the sacrificial layer using a photoresists material, that is later removed, as a mask (item 1) and patterning the hard mask layer

using the photoresist material and the sacrificial layer as masks (Fig. 1E and/or 8E) so as to form a first sacrificial layer pattern having an opening that crosses over the via hole and a second sacrificial layer patter that remains in the via hole (See Figs. 1E and/or 8E) and to simultaneously form a hard mask pattern underneath the first sacrificial layer pattern (Figs. 1E and/or 8E) and etching the upper intermetal dielectric layer (item 4) using the hard mask pattern and the sacrificial pattern as etching masks (Fig. 1F and/or 8F) to form a trench crossing over the via hole and removing the second sacrificial layer pattern to expose the lower interconnection line. (Fig. 1G and/or 8G)

It would have been obvious to one having ordinary skill in the specific art to combine the teachings of Nagahara et al. to the invention of Chung et al., since Chung et al. teaches multiple layers of dielectric material, since Nagahara et al. teach a well known process of forming damascene structures that will result in a controlled and desired formation of the trench and via hole and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. Furthermore, both Nagahara et al. and Chung et al. are directed to achieving a the same structure and thus one with ordinary skill in the specific art would recognize the interchangeability of the process steps and be able to combine the two inventions with an expectation of success.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,383,912 B1 (Chung et al.) in view of US Patent No. 6,514,852 B2 (Usami).

As stated in paragraph 4, all the limitations of the claim have been met except for

teaching that the dielectric layer is only one.

Usami teaches the formation of a damascene structure wherein a via is first formed and then a sacrificial layer is deposited in the via and wherein the trench is then patterned, wherein the dielectric layer may be only one layer. (Fig. 1E-1F).

It would have been obvious to one with ordinary skill in the specific art to combine the prior art teachings disclosed in Usami with the invention of Chung et al., since it has been held that constructing formerly various elements into an integral structure involves only routine skill in the art. *Howard v. Detroit Stove Works*, 150 US 164.

10. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,383,912 B1 (Chung et al.) in view of US Patent Publication No. 2003/0157806 A1 (Nagahara et al.) and in further view of US Patent No. 6,573,168 (Kim et al.)

As stated in paragraph 8, all the limitations of this claim have been met except for teaching the deposition of an antireflective coating on the sacrificial layer.

Kim et al. teach depositing an ARC layer over an HSQ layer prior to depositing a photoresist layer. (col. 6, lines 10-25).

It would have been obvious to one with ordinary skill in the specific art to form an ARC layer over the HSQ layer, since Kim et al. teach that the use of an ARC layer will result in more precise patterning. (Kim et al., col. 6, lines 10-25).

11. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Publication No. 2003/0157806 A1 (Nagahara et al.) in view of US Patent No. 6,573,168 (Kim et al.)

As stated in paragraph 5, all the limitations of this claim have been met except for teaching the deposition of an antireflective coating on the sacrificial layer.

Kim et al. teach depositing an ARC layer over an HSQ layer prior to depositing a photoresist layer. (col. 6, lines 10-25).

It would have been obvious to one with ordinary skill in the specific art to form an ARC layer over the HSQ layer, since Kim et al. teach that the use of an ARC layer will result in more precise patterning. (Kim et al., col. 6, lines 10-25).

12. Claims 29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Publication No. 2003/0157806 A1 (Nagahara et al.) in view of US Patent No. 6,383,912 B1 (Chung et al.).

As stated in paragraph 5, all the limitations of this claim have been met except for specifying that the hard mask layer is formed of a conductive metal nitride and that a barrier layer is deposited in the via and trench prior to the metal layer.

Chung et al. teach that the hard mask may comprise a metal nitride such as titanium nitride. (col. 10, lines 31-39) and that the via and trench are filled with a metal and a diffusion barrier layer and the metal is then planarized. (Fig. 2J).

It would have been obvious to one with ordinary skill in the specific art to combine the teachings of Chung et al. to the invention disclosed by Nagahara et al., since the barrier layer will prevent the diffusion of the metal ions into the dielectric layer

that would cause leakage current and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Renzo N. Rocchegiani whose telephone number is (571)272-1904. The examiner can normally be reached on Mon.-Fri. 8:00 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571)272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Renzo N. Rocchegiani
Examiner
Art Unit 2825

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800